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RECTIFIER

COMPONENTS

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QUARTERLY PROGRESS REPORT

FOR

THE RESEARCH AND DEVELOPMENT

OF

HIGH CURRENT AND HIGH VOLTAGE

SILICON CONTROLLED RECTIFIERS

THIS REPORT COVERS THE PERIOD

1 October 1962 TO 31 December 1962

RECTIFIER COMPONENTS DEPARTMENT

GENERAL ELECTRIC COMPANY

WEST GENESEE STREET

AUBURN, NEW YORK

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISIONS

CONTRACT NUMBER: NObsr-87648

PROJECT SERIAL NUMBER: SF-013-11-05

CONTRACT DATE: 30 JUNE 1962

ABSTRACT

The second quarterly progress report for the research and development of high-current and high-voltage, silicon controlled rectifiers under the Navy Department Contract Number NObsr-87648, Project Serial Number SF-013-11-05 of 30 June 1962, covers the work performed on Device B and Device C of the subject contract during the period of 1 October 1962 through 31 December 1962. The status of fabrication of Device B state-of-the-art samples is reported herein; also discussed is the progress in the optimization of parameters for this device. A program for a computer calculation of depletion region width of a p-n junction is also described. The developments in the design of Device C are included.

PART I

1.1 PURPOSE

This second quarterly progress report covers the effort applied to Project Serial Number SF-013-11-05 during the period of 1 October 1962 through 31 December 1962. The purpose of this program is to design, develop and produce devices capable of meeting the requirements specified under the Navy Department, Bureau of Ships Contract Number NObsr-87648, "Research and Development of High-Current and High-Voltage Silicon Controlled Rectifiers". The progress reported herein is written in two (2) sections; the first covers Device B and the other section, Device C.

2.1 GENERAL FACTUAL DATA

2.1.1 Identification of Technical Personnel

The names of engineers and engineering technicians, together with a summary of the manhours of work performed for each device, are as listed below:

(a). Device B

Engineers	Technicians
R. Kennedy	M. C. Brown
R. Knaus	K. B. Catchpole
R. H. Werner	M. H. Curtin
	J. Kellam
	M. H. Lindner
	J. Metroka
	E. Roberts
	A. L. Smith

(b). Device C

Engineers	Technicians
R. L. Davies	A. Bolger
R. Kokosa	J. Brunner
R. P. Lyon	J. B. Crooks
S. S. Shaffran	J. Kimball
	B. Tuft
	M. Yaworsky

(c). Manhours

Engineers	Technicians
1960	3492

2.1.2 References

(1). Quarterly Progress Report, "The Research and Development of High Current and High Voltage Silicon Controlled Rectifiers", for the period 30 June 1962 through 30 September 1962. Prepared by the Rectifier Components Department of the General Electric Company for the Navy Department, Bureau of Ships, Electronics Divisions, Contract Number NObsr-87648, Project Serial Number SF-013-11-05, Contract Date: 30 June 1962.

2.1.3 Illustrations

All illustrations referenced in PART I of this quarterly report are appended to PART III of this report.

3.1 DETAIL FACTUAL DATA

3.1.1 Device B

3.1.1.1 Statement of the Problem

This section of the detail factual data covers Device B which is basically a 1000 volt, 70 ampere, silicon controlled rectifier in the JEDEC Registration Number Series, 2N1909 - 2N1916. The design required is a large area PNPN structure with a very high voltage capability.

To obtain the full operating voltage theoretically possible by device design, it is necessary to overcome surface field effects which have limited present day PNPN devices to well below the 1000 volt rating desired. These field dependent effects are a function of the gross imperfections and electric field concentration at the silicon surface-dielectric interface, and limit the voltage capabilities of the device by resulting in surface avalanche rather than a theoretical bulk breakdown. The use of a properly contoured surface will diminish both the imperfections and the field concentration, resulting in full utilization of device capability and also a more stable device which will be free of destructive surface effects.

A second, very important problem is in impurity precipitation and segregation effects in the silicon. It has become of more significance as a result of the ability to suppress surface avalanche. With the attainment of control of the surface field, this problem has become dominant and is hampering the optimization of design parameters. These effects occur during the diffusion and alloying processes, and are causing excessive reverse leakage currents which make it difficult to obtain theoretical bulk breakdown voltages.

Effort is being concentrated in obtaining a solution to this problem so that production of high-voltage devices is possible with reasonable yields.

A third problem, and one that is very much inter-related with the other two problems, is the choice of practical device geometry and impurity distributions so that the desired breakdown voltages are obtained without seriously affecting other device characteristics. In fact, to meet the requirements of the contract, one parameter -- turn-off time -- must be improved over the present standard device. In addition, this must be done within a package that meets the outline of the JEDEC No. 2N1909 - 2N1916 Series.

3.1.1.2 Approach to the Problem

Refer to Figure 1, PART III, for Device B structure and contour design. The initial junction design was derived by consideration of the theoretical bulk breakdown of silicon, and the resistivity and geometry required to obtain bulk avalanche at the required voltage. To insure an operating voltage of 1000 volts, an avalanche breakdown voltage was chosen between 1200 and 1300 volts. The base concentration of $1.6 - 1.8 \times 10^{14}$ corresponding to this breakdown voltage was obtained from Figure 6 - Avalanche Breakdown in PN Junctions, found in PART III of the Quarterly Progress Report for the period 30 June 1962 through 30 September 1962. The width of the N-region of Device B was selected so that, when either the reverse or forward junction is biased at voltages up to avalanche breakdown voltages, the respective depletion regions do not spread entirely across the N-region resulting in "punch-through" breakdown and poor high temperature characteristics. The barrier spread corresponding to the base concentration chosen is 4.5 mils and is taken from Figure 7 - Barrier Width in a PN Step Junction at Avalanche Bias, of the Quarterly Progress Report referred to above.

To insure operation in the avalanche region, a base width of 5.5 mils was originally chosen (Refer to 3.1.1.3). The values for the P-region thickness and surface concentration (3 mils and $1x10^{18}$) were chosen after consideration of the practicality of the diffusion cycles required, the resulting effectiveness of the contour surface at the forward junction, and the resulting forward voltage drop in the conducting state. A thick P-region increases the effectiveness of the contour but requires excessive diffusion cycles. A low, surface concentration enhances the effectiveness of the contour but increases the forward voltage drop. The pellet diameter of 700 mils was chosen to obtain the desired average forward current as determined by the emitter area and an effective surface contour.

In order to obtain bulk avalanche, as opposed to surface avalanche, and stable operation at these high voltages, the surface field should be lowered as much as is practically possible below the bulk field at each junction. This is being accomplished by surface contouring. The most successful method of surface contouring is a mechanical process that produces a bevel at the edge of a round pellet and at a specified angle. It is relatively easy to perform this process in the laboratory, or on the manufacturing line, and is very practical because of the accurate control over the angle or angles required. Since the peak surface field along the contour for the forward junction is higher than that of the reverse junction, this method allows the use of an optimum angle for each individual junction via a double bevel (two-step process) without unnecessary waste of the pellet diameter. Based on previous experience with surface contouring, a small angle (from the plane of the junction) was projected as being required to lower the peak surface field at the forward junction below that which is considered critical for controlled-avalanche type devices. Since the peak surface field along the contour of the reverse junction is lower than that of the forward junction, a higher angle can be used. The larger angle was chosen because it was necessary to remain within the allowed diameter of the pellet.

To some extent the poisoning effects of unwanted impurities in the silicon, as evidenced by the softening of blocking voltage current characteristics, has been kept under control by careful control of processing techniques and careful cleaning of parts, fixtures and oven used during diffusion and alloying, and by proper gas control during these operations. This problem has occurred often enough to hamper the optimization of some parameters of this device. The problem is being approached in parallel studies to either eliminate the introduction of these impurities into the device by alterations in the processing techniques, or to find a method of removing the impurities (such as impurity gettering or precipitation in a harmless form).

In order to meet the requirements of some parameters such as, voltage rate of rise, and turn-off time, close control of lifetime is required by means of gold diffusion. This must be done without seriously impairing high-current forward drop, turn-on time, and trigger currents. A lifetime level must be established to maintain the proper balance of the device parameters affected.

3.1.1.3 Optimization of Design Parameters

The optimization of the base resistivity and device geometry to obtain the desired operating voltage has resulted in the choice of a minimum base resistivity of 40 ohm-cm. Specifications for the purchase or growth of the necessary N-type silicon have been set at minimum practical limits of 40 - 50 ohm-cm. Data from the computer program for calculation of barrier spreading (This will be discussed in section 3.1.2 Device C of this report.) indicated that a base width of 5 mils is necessary to prevent "punch-through" at these resistivities. The minimum for the base width was reset at 6.5 mils which includes an allowance of 1.5 mils to minimize elevated temperature leakage currents caused by transistor action.

Results from the completed computer study on junction contouring (as discussed in Section 3.1.2 - Device C of First Quarterly Progress Report) showed that the peak surface field along the contour at the forward junction is minimized with the use of an angle somewhat larger than that originally projected. To optimize the effect of the beveled contour, the angle across the forward junction was changed to the larger value. The saving on the diameter as a result of this change was used to advantage in changing the angle of the bevel across the reverse junction to a smaller angle. Losses by chipping of the edge of the silicon pellet are diminished at the lower angle. This loss is also minimized by using a pellet cutting technique which gives a tolerable square edge to the pellet, and by using an extremely thin layer of aluminum as the contact material between the pellet and the bottom contact plate.

The base lifetime level to meet all parameter requirements has not been established. Results to date indicate that lifetime control is needed to meet the turn-off time specification, but not the dv/dt specification. The high-current forward voltage drop is being affected more seriously than the trigger current. Some of the forward voltage drop increase may be a result of the impurity problem discussed above.

3.1.1.4 State-Of-The-Art Sample Fabrication

Junction assembly components have been designed, procured and used for the initial (state-of-the-art) design samples. The initial geometry and contour of the junction structure have been modified as information has been obtained during optimization of design parameters. No change in components was necessary, but some modifications to the original fixtures, tools and jigs were made as a result of the device changes. Samples were prepared representing the state-of-the-art at this time, and are being electrically evaluated for delivery as scheduled.

3.1.2 Device C

3.1.2.1 Junction Assembly Work

In order to evaluate the effectiveness of the surface contour on both the VBO and PRV junctions of Device C, a group of PNP pellets were gallium diffused. These structures had a surface concentration of $1x10^{18}$, a P diffusion depth of 4 mils, base resistivity of 40 - 45 ohm-cm, and a base width of 6.5 mils. The pellet diameter was compatible with the required current rating for Device C.

The method for surface contouring was a mechanical process that applied a bevel at the edge of a round pellet and at a small angle extending slightly beyond the PRV junction.

Electrical evaluation confirmed that the peak field existing along the surface of a reverse-biased junction was reduced, and that theoretical avalanche voltage breakdown was observed on both the VBO and PRV junctions.

It became evident while working with these structures that future work with a single bevel would not be practical, and a double bevel consisting of a small angle and a larger angle would be required to conserve silicon.

In the change from the single bevel to the double bevel, a fracturing problem was encountered. While beveling the larger angle, severe fracturing of the pellet edge occurred. It was then necessary to change the pelletizing process to one that insured a 90° angle at the bottom of the pellet edge. There was more back-up support at the periphery of the silicon pellet by using this straight edge process of pelletizing; thus eliminating the fracturing problem.

Preliminary evaluation of four (4) diffusion runs indicate a greatly reduced peak electric field on the VBO junction surface. In all but one diffusion run, theoretical avalanche voltage breakdown was observed on both the VBO and PRV junctions. This one diffusion run indicated a "punch-through" due to a narrow base width.

In attaching back-up plates to these all-diffused structures, a thin layer of aluminum was used as the mounting solder for both the PRV and VBO sides. Fixtures for the precise placement of the aluminum with respect to the emitter were designed and built. This precise placement is a requirement for effective emitter shorting.

3.1.2.2 Surface Contour and Geometry Work

The three surface contours proposed in the First Quarterly Progress Report for this Bu Ships Project were tried. As was hoped, all three contours gave high-voltage characteristics. However, a design very similar to that depicted in Figure 5 of the above report was determined to be the best at this time. Minor changes in the parameters of this design became necessary for overall process compatibility.

Values of resistivity between 40 and 50 ohm-cm give 1400 to 1500 volts avalanche. The surface concentrations shown are compatible with the double-diffusion process developed by the Rectifier Components Department for an all-diffused, silicon-controlled rectifier. The completed pellet yields the voltage capability indicated in Figure 2 (PART III of this report). The forward drop of these devices at 1500 amperes was approximately 2.5 volts. The gate sensitivity, depending upon the type of emitter shorts used, was 50 to 300 milliamperes.

The high-temperature, VBO blocking characteristic on some devices was similar to that indicated by the dashed curve in Figure 2 of this report. The reason for the high current in this direction was found to be due to poor emitter shorting at the periphery of the

emitter. A suitable method of shorting the emitter periphery while maintaining a good gate sensitivity is being worked out.

3.1.2.3 Calculation of Depletion Region Width

During the fabrication of a PNP (or NPN) structure by deep diffusion, the diffusion "tails" from both sides of the wafer cause compensation of impurities in the base as shown in Figures 3a and 3b of this report. If the junction, J_1, is reverse-biased and it is desired to calculate the width of the depletion region for applied voltages near that of "punch-through", the assumption of a step-function impurity distribution is no longer valid. As a result, a General Electric 225 Computer was programed to calculate the depletion region width for any impurity distribution.

The voltage distribution in the depletion region of a reverse-biased, PN junction is described by Poisson's Equation, as follows

$$\nabla^2 V = \frac{-\eta(x)}{\epsilon} \qquad (1)$$

where, $\eta(x) = q(N_d - N_a)$. It will be assumed that the voltage distribution across the junction in question is unaffected by surface conditions. The boundary condition of this problem is that, at the edges of the depletion region, the electric field intensity must be zero (0). Since the PNP structure is fabricated by gallium diffusion into a wafer of constant resistivity, the donor concentration, N_d, is a constant with respect to x and the acceptor concentration, N_a, is specified by a complementary error function diffusion from both sides of the wafer, so that

$$(N_d - N_a) = N_d - C_o \left[\mathrm{ERFC}\left(\frac{x}{2\sqrt{Dt'}} \right) + \mathrm{ERFC}\left(\frac{W - x}{2\sqrt{Dt'}} \right) \right] \qquad (2)$$

Thus, from the form of Equation (2), it is shown that Equation (1) is intractable in closed form and that the solution to $\underline{V}$ must be found by numerical means.

Assume that a one-dimensional array of nodes is across the PNP wafer in the x direction, then from Appendix A (PART III, this report) the finite difference approximation to Poisson's Equation at the n^{th} node becomes

$$V_{n-1} + V_{n+1} - 2V_n + \frac{h_n^2 \eta(n)}{\epsilon} = 0. \tag{3}$$

From this equation we define the residual at the n^{th} node as

$$R_n = V_{n-1} + V_{n+1} - 2V_n + \frac{h_n^2 \eta(n)}{\epsilon}. \tag{4}$$

With this equation, the solution to Poisson's Equation may be approximated at each node point by demanding that R_n be less than $\mathcal{E}$, where $\mathcal{E}$ is some small voltage which causes the assumed voltage distribution to converge to a voltage distribution which is a solution to Poisson's Equation.

The computer program for this problem is described, briefly, by the flow chart of Figure 6 (PART III). Further explanation of the input data and of the calculation of the voltage distribution would be advantageous to the understanding of the program. This input data consists of the wafer thickness, the number of nodes to be used, the applied voltage, and twenty (20) values of $(N_d - N_a)$ with their corresponding positions within the wafer.

In order to simplify the programming of Equation (4), a normalized voltage of 1000 was used. The normalized voltage, V_n, at the n^{th} node is defined as $V_N' = aV_n$, where $a = 1000/V_{app}$. Thus, Equation (4) becomes

$$R_n' = V_{n-1}' + V_{n+1}' - 2V_n' + \frac{ah_n^2 \eta(n)}{\epsilon}. \tag{5}$$

Now, the term $\rho_n' = \frac{ah_n^2 \eta(n)}{\epsilon}$ is defined as a normalized density and contains the input data of Equation (5). Thus, Equation (5) becomes

$$R_n' = V_{n-1}' + V_{n+1}' - 2V_n' + \rho_n' \quad (6)$$

Although the function $\eta(n)$ may vary by a factor of 10^4, depending upon its position within the wafer, the function ρ_n varies by a factor of less than 4. This is due to the fact that the table of node spacings is chosen in such a manner that, as the impurity density decreases by a factor of 4, the node spacing increases by a factor of 2, and vice-versa.

The calculation of the true voltage distribution across the junction begins with the assignement of a normalized voltage to each node. Unless a better voltage distribution is known, a linear voltage distribution is assigned. After this is done, each node is tested in the following manner: the electric field, E_n, at the node is calculated and compared to a small test field, E_o. If $E_n \leq E_o$, then the node is outside of the space charge region and the voltage at that node is set to either zero (0) or 1000 depending upon which side of the junction the node is located. If $E_n > E_o$, the residual, R_n, is calculated. If $|R_n| < |\mathcal{E}|$, then the voltage at the node is left unchanged. If $|R_n| > |\mathcal{E}|$, than a factor of $R_n/2$ is algebraically added to the voltage of the node in question. If the voltage at any node is changed during this process then the voltages of adjacent nodes are tagged, which means that their voltages must be retested. This continues until the calculated voltage distribution is one which satisfies Poisson's Equation within the limits of the test parameters, E_o and $\mathcal{E}$. It should be noted that some nodes do exist which have node spacings on either side which are not equal. In this case, the finite difference approximation to Poisson's Equation is not valid and a further approximation is necessary.

Design parameters for both Device B and C were inserted into this program. Both of the devices use a base resistivity range of 40 to 50 ohm-cm, and a gallium surface concentration of approximately

1.10^{17} atoms/cm^3. Using this data in conjunction with Equation (2), the twenty (20) input impurity density points were calculated for various wafer widths, W, and inserted into the computer program. The results are shown in Figures 4 and 5 for base resistivities of 40 to 50 ohm-cm and for applied voltages of 1200 and 1500 volts. These curves indicate how far the depletion region spreads into N-type base as a function of the base width.

With reference to Figure 5 it is seen that "punch-through" is greater in PNP structures by an increase in base resistivity (i.e., the effect of diffused compensation upon "punch-through" is greater for high resistivity bases). The curves, Figures 4 and 5, show that the maximum effect of diffused compensation upon the depletion region spreading is restricted to approximately 0.4 mils in the devices under consideration. Therefore, if the simple spreading curve as shown in the First Quarterly Report is used, an additional 0.4 mils must be added when determining the barrier width. Previous estimates of this factor varied from 0.25 to > 1 mil because of the high resistivities involved.

A complete list of symbols as used in this analysis is included in Appendix A, PART III of this report.

3.1.2.4 High-Voltage and High-Current dV/dt Test Equipment

Construction of the high-voltage, dV/dt test equipment is being continued. All parts have been obtained so that no further delay in its construction is expected.

3.1.3 Project Performance and Schedule Chart

An up-to-date project performance and schedule chart for the period covered by this report on Project Serial No. SF-013-11-05 will be found on the following page.

RECTIFIER COMPONENTS DEPARTMENT

GENERAL ELECTRIC

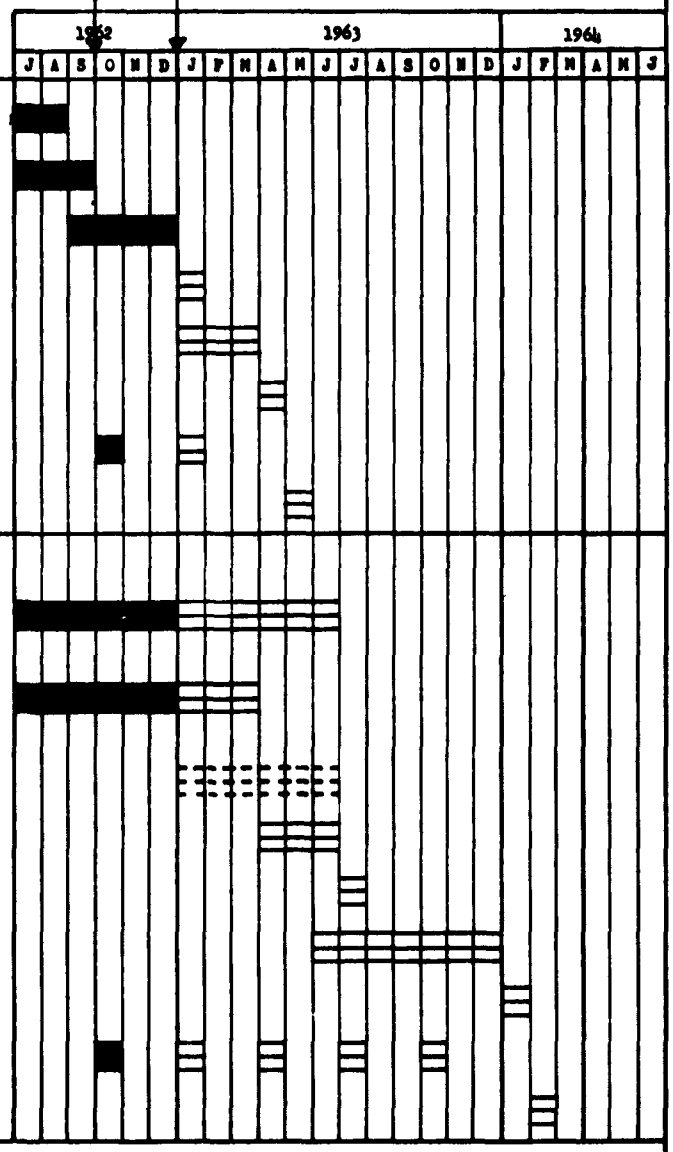
AUBURN, NEW YORK

PROJECT PERFORMANCE AND SCHEDULE

PROJECT SERIAL NUMBER: SF-013-11-05

CONTRACT NUMBER: NObsr-87648 (REPORT) DATE: 31 January 1963

PERIOD COVERED: 1 Oct to 31 Dec 1962



LEGEND: ▬ - WORK PERFORMED

▭ - SCHEDULE OF PROJECTED OPERATION

ITEM: ESTIMATED COMPLETION IN PERCENT OF TOTAL EFFORT EXPECTED TO BE EXPENDED (NOT CHRONOLOGICAL).

1. DEVICE B - 60 %

2. DEVICE C - 35 %

NOTES AND REMARKS:

PART II

4.1 PROGRAM FOR THE NEXT QUARTER

4.1.1 Device B

Optimization of the remaining design parameters will be completed with emphasis on obtaining and maintaining an optimum lifetime. State-of-the-art samples will be evaluated and delivered. Fabrication and evaluation of final design units will occupy most of the effort during the next quarter.

4.1.2 Device C

Further work in diffusion and contacts will proceed. Emphasis will be placed upon shorted emitter design and upon measurement of other parameters such as, turn-off time, forward drop, and dV/dt. Further modification of the structure may be necessary to enable optimization of the above parameters.

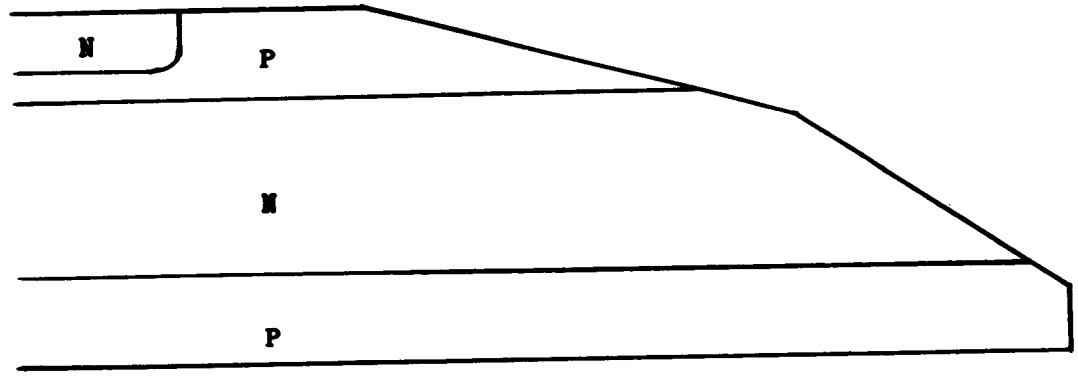


Figure 1 - Device B structure and contour design

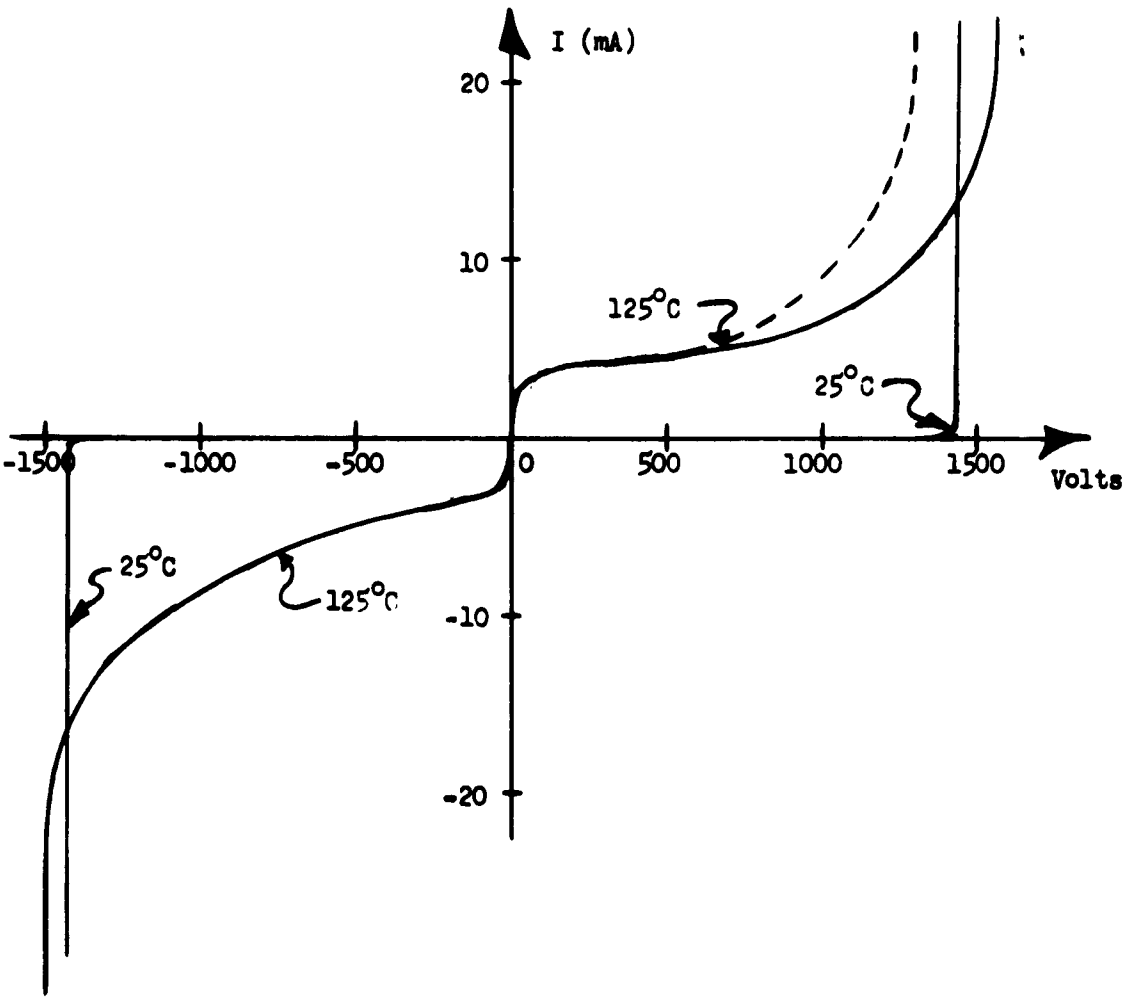


Figure 2 - Device C characteristics

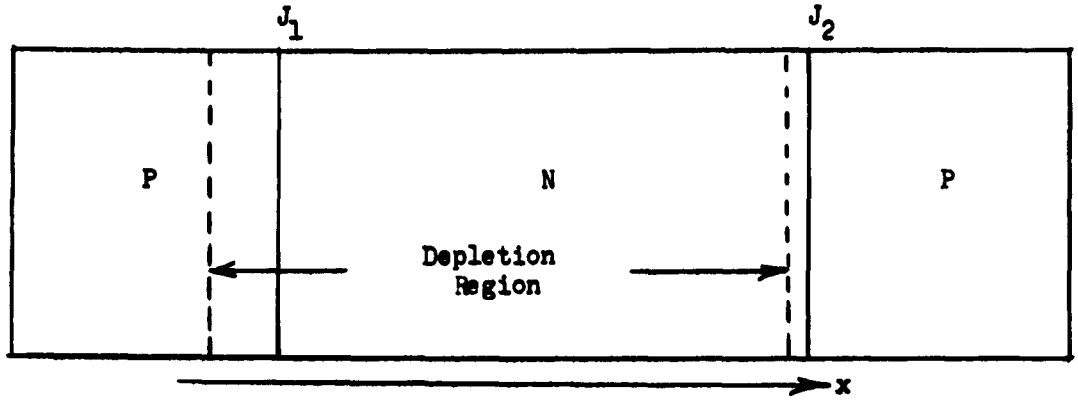


Figure 3a - Device cross section

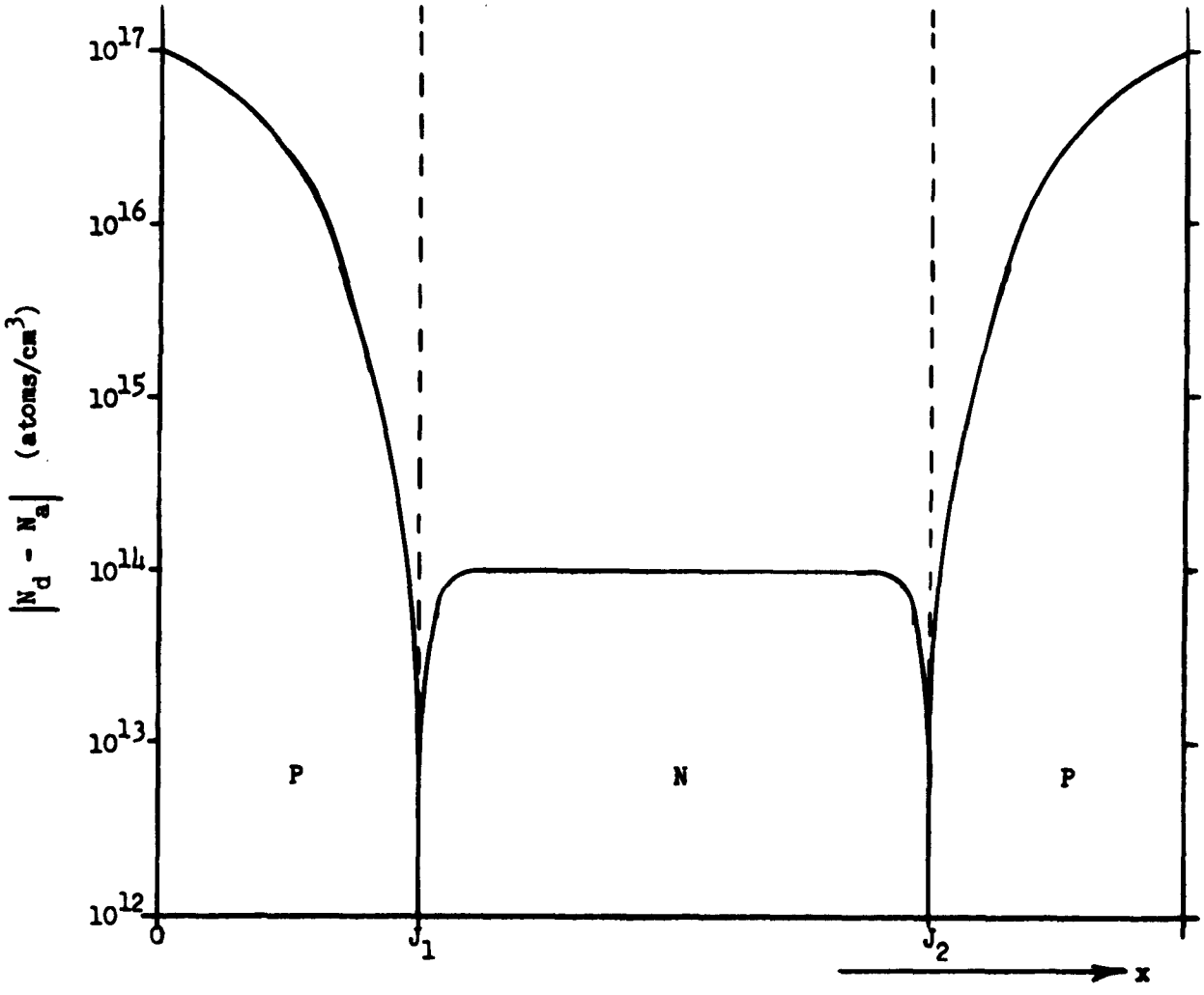


Figure 3b - Impurity distribution

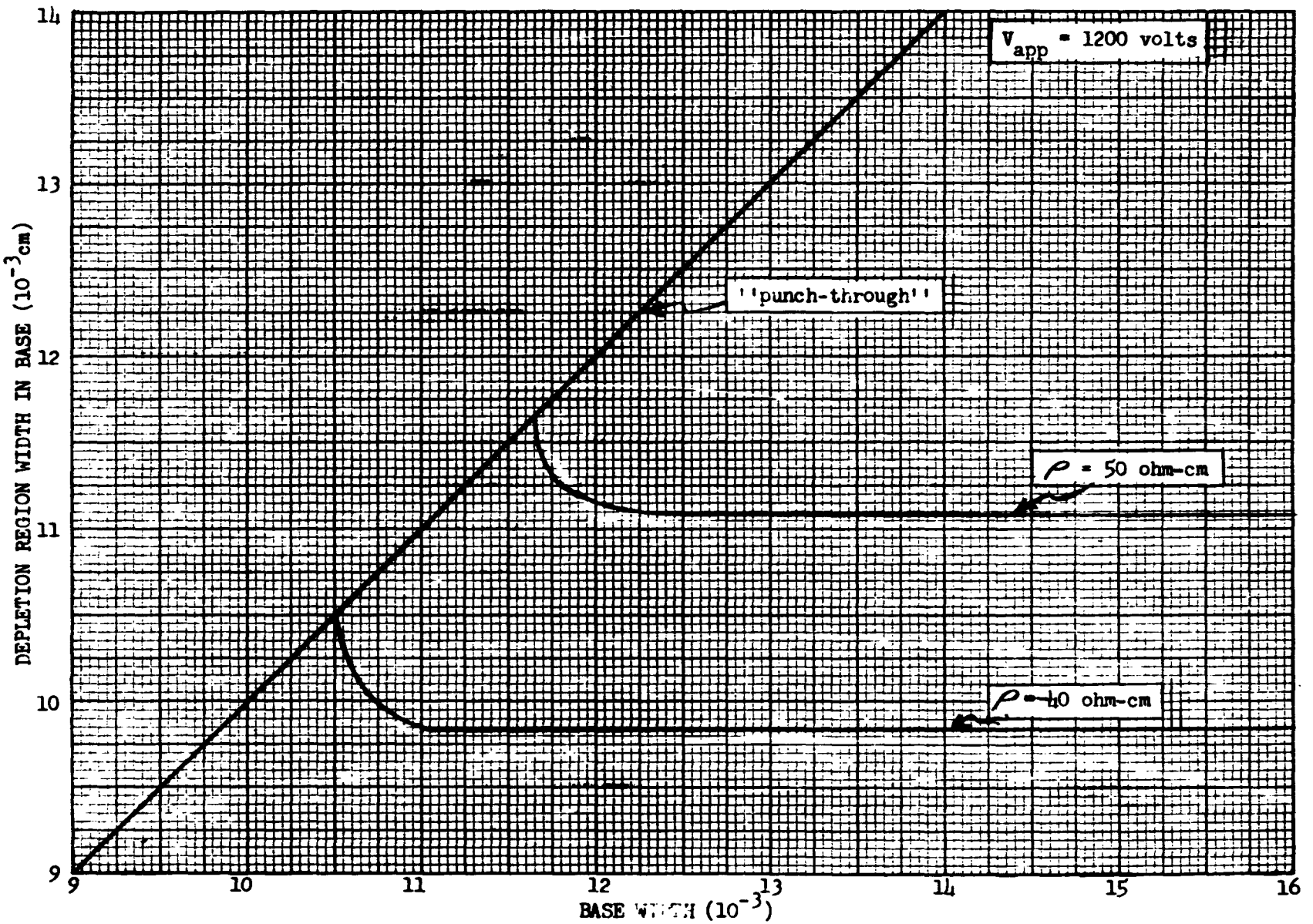


Figure 4 - Base width design

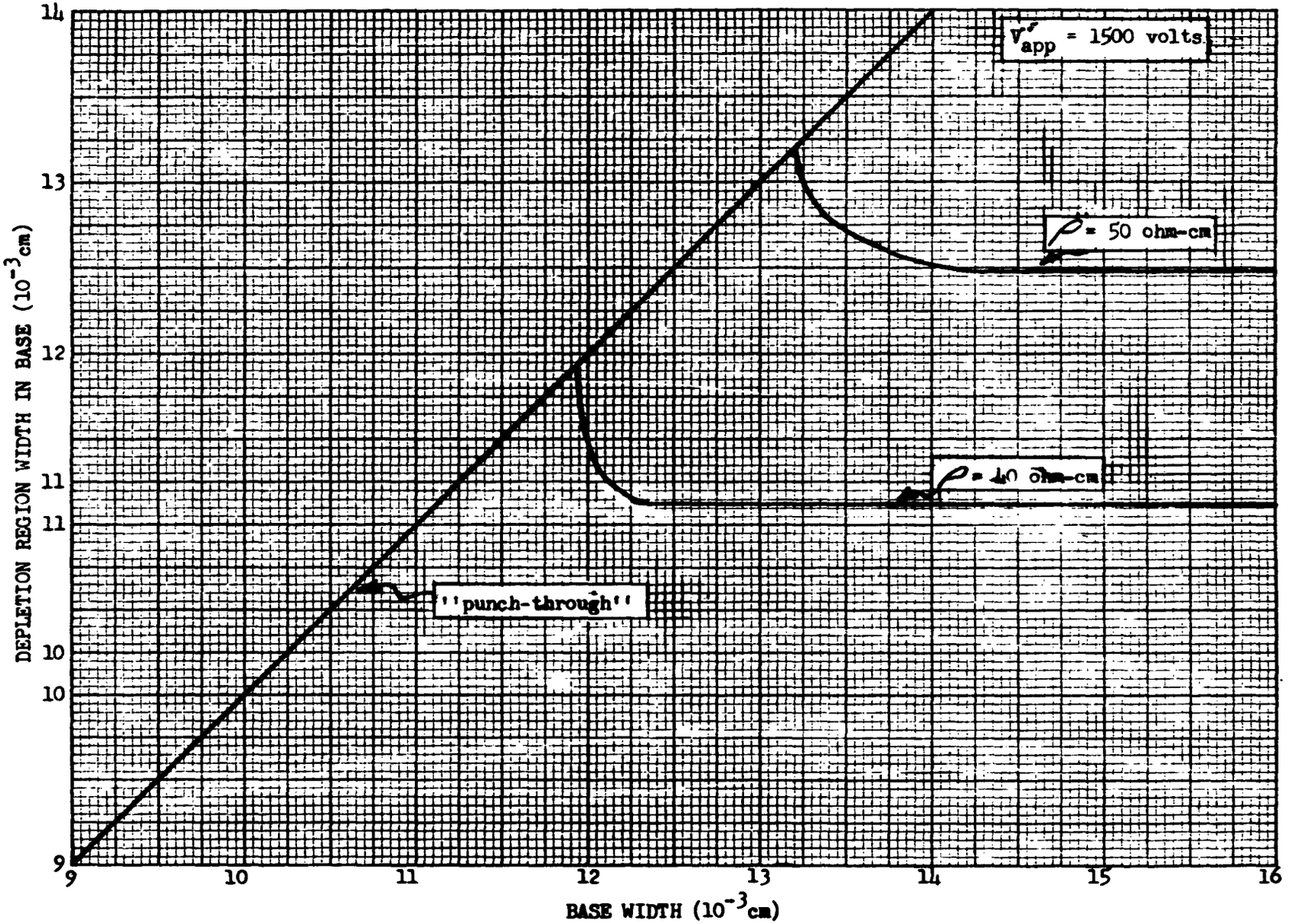


Figure 5 - Base width design

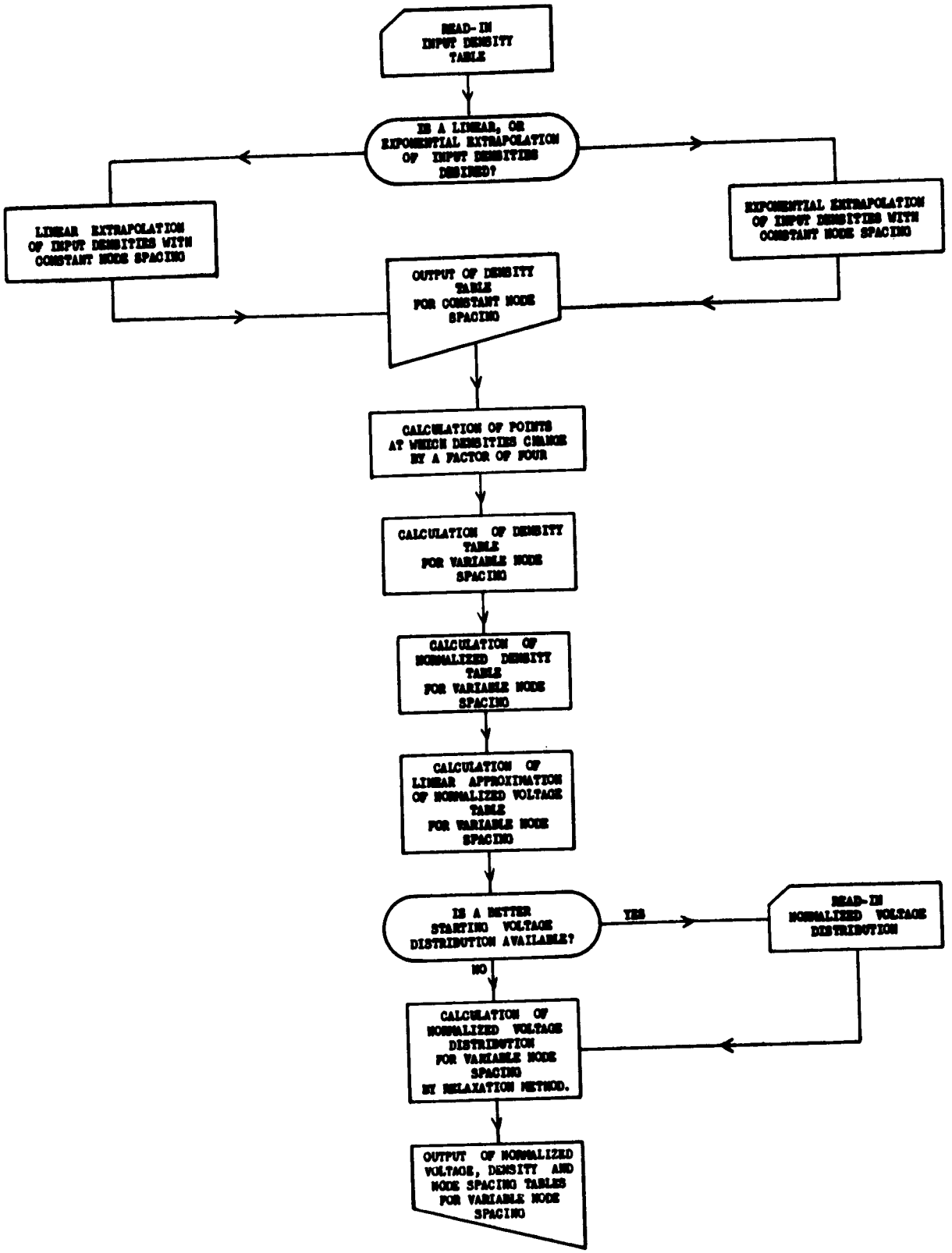


Figure 6 - Flow chart of barrier width program

APPENDIX A

FINITE DIFFERENCE APPROXIMATION TO POISSON'S EQUATION

In one dimension Poisson's Equation states that

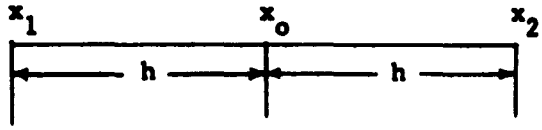
$$\frac{\partial^2 V}{\partial x^2} + \frac{\eta(x)}{\epsilon} = 0. \tag{A1}$$

Performing a Taylor series expansion around the point $x=x_o$ on the above equation results in

$$V = V\Big|_{x=x_o} + \left(\frac{\partial V}{\partial x}\right)\Big|_{x=x_o} (x - x_o) + \frac{1}{2!}\left(\frac{\partial^2 V}{\partial x^2}\right)\Big|_{x=x_o} (x - x_o)^2 +$$

$$\frac{1}{3!}\left(\frac{\partial^3 V}{\partial x^3}\right)\Big|_{x=x_o} (x - x_o)^3 + \frac{1}{4!}\left(\frac{\partial^4 V}{\partial x^4}\right)\Big|_{x=x_o} (x - x_o)^4 + \ldots\ldots\ldots \tag{A2}$$

Consider the point $x=x_o$ as a node in a one-dimensional system of nodes spaced h distance apart as indicated below:



Then, by writing Equation (A2) for the points $x=x_1$ and $x=x_2$, it is found that

$$V_1 = V_o - h\left(\frac{\partial V}{\partial x}\right)\Big|_{x=x_o} + \frac{h^2}{2!}\left(\frac{\partial^2 V}{\partial x^2}\right)\Big|_{x=x_o} - \frac{h^3}{3!}\left(\frac{\partial^3 V}{\partial x^3}\right)\Big|_{x=x_o} +$$

$$\frac{h^4}{4!}\left(\frac{\partial^4 V}{\partial x^4}\right)\Big|_{x=x_o} + \ldots\ldots\ldots\ldots$$

and,

$$V_2 = V_o + h\left(\frac{\partial V}{\partial x}\right)\Big|_{x=x_o} + \frac{h^2}{2!}\left(\frac{\partial^2 V}{\partial x^2}\right)\Big|_{x=x_o} + \frac{h^3}{3!}\left(\frac{\partial^3 V}{\partial x^3}\right)\Big|_{x=x_o} +$$

$$\frac{h^4}{4!}\left(\frac{\partial^4 V}{\partial x^4}\right)\Big|_{x=x_o} + \ldots\ldots\ldots\ldots$$

where $V_o = V\big|_{x=x_o}$, $V_1 = V\big|_{x=x_1}$, and $V_2 = V\big|_{x=x_2}$.

Addition of the above equations results in

$$V_1 + V_2 = 2V_o + h^2\left(\frac{\partial^2 V}{\partial x^2}\right)\Big|_{x=x_o} + O(h^4).$$

Therefore, for a very small node spacing $\underline{h}$

$$h^2\left(\frac{\partial^2 V}{\partial x^2}\right) = V_1 + V_2 - 2V_o \qquad \text{(A3)}$$

And by substituting Equation (A3) into Equation (A1), Poisson's Equation becomes

$$V_1 + V_2 - 2V_o + \frac{h^2\,\eta(x)}{\epsilon} = 0. \qquad \text{(A4)}$$

SYMBOL LIST FOR CALCULATION OF DEPLETION REGION WIDTH

$V = V_{(x)}$ = Voltage at a point x in the voltage distribution.

V_{app} = Applied voltage across the junction.

$N_d = N_{d(x)}$ = Concentration of donor impurities (at point x).

$N_a = N_{a(x)}$ = Concentration of acceptor impurities (at point x).

q = Electronic charge.

ϵ = Dielectric permittivity.

$\eta(x)$ = Net fixed charge density at a point x.

h_n = Node spacing between the n^{th} and $(n - 1)^{th}$ nodes.

$\eta(n)$ = Net fixed charge density at the n^{th} node.

V_n = Voltage at the n^{th} node.

R_n = Residual of Poisson's Equation at the n^{th} node.

R_n' = Normalized version of R_n.

V_n' = Normalized version of V_n.

E_n = Electric field intensity at the n^{th} node.

E_o = Test value of electric field intensity for computer program.

$\mathcal{E}$ = Test value of normalized voltage for computer program.

W = Width of wafer.

C_o = Surface concentration of diffusing impurity.

D = Diffusion constant of diffusing impurity.

t = Diffusion time.

ERFC = Complementary error function.